1 kW, Multi-MHz Wireless Charging for Electric Transportation

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***Abstract*—We design and build a DC-DC wireless power system for electric vehicles charging at 6.78 MHz. With a gap of 34 cm, the air-core system can transfer up to 1 kW with 82% efficiency. It can operate continuously without failure even when the gap varies from 26 to 38 cm, and though the output power changes with distance, the efficiency does not vary appreciably. Due to the high operating frequency, the transfer coils are lightweight, inexpensive, and mechanically robust, even with a gap much larger than in previous literature. The system's low cost and resilience across coupling makes it amenable to mass deployment in commercial systems.**

Keywords—Wireless power transfer, automotive charging, electric vehicles, matching networks.

I. Introduction

The on-road transportation fleet will likely transition to electric propulsion in the next 5–10 years, catalyzed by an enormous reduction in total cost of ownership for electric vehicles (EVs) relative to internal combustion engines. However, the electric fleet will impose a large stress on the U.S. grid infrastructure, with most of the electricity demand added at peak hours. A wireless charging system that could recharge vehicles on the road could decentralize energy demand both temporally and spatially, enabling a cleaner transition to electric vehicles.

Existing wireless power transfer systems have coalesced around the Society of Automotive Engineers (SAE) standard at 85 kHz. However, at this frequency, the magnetic materials and large coils needed to obtain reasonable efficiencies add enormously to the weight and cost of the chargers. We propose to move to a much higher frequency of 6.78 MHz and eliminate the expensive ferrites and litz wire of the low-frequency designs. Existing wireless power systems at high-frequency (> 3 MHz) and large gap (> 30 cm), however, do not achieve high efficiencies or kW-scale power levels [1-6], and a demonstration of the feasibility of kW-scale, MHz chargers for EVs is needed. In this paper, we design and demonstrate a DC-DC wireless power transfer system operating at 6.78 MHz capable of transferring 1 kW of power over a gap of more than 30 cm.

II. Power Inverter

A. Switch Selection and Load Design

The inverter uses a half-bridge Class D configuration, as shown in Fig. 1a. The switches are GS66508T GaN high-electron-mobility-transistors (HEMTs) [7]. The inverter takes a 400 V supply and should be able to deliver up to 1.1 kW. To design the load, we use the standard formula for Class-D architectures [8]:

$$P_{out}=\frac{2}{\pi^2}\frac{V_{DD}^2}{|Z_L|}\cos(\phi) \tag{1}$$

Using a conduction angle of ϕ = 45° for a good zero-voltage-switching (ZVS) margin, the magnitude of the load impedance seen by the inverter should be $|Z_L| < 21\ \Omega$. We use a parallel LC matching network to transform a standard 50 Ω

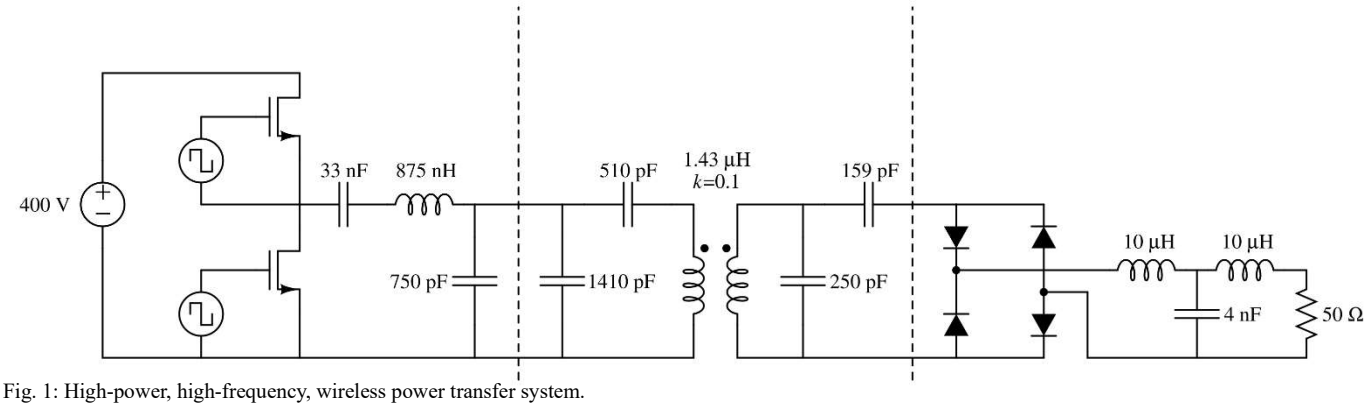

Fig. 1: High-power, high-frequency, wireless power transfer system.

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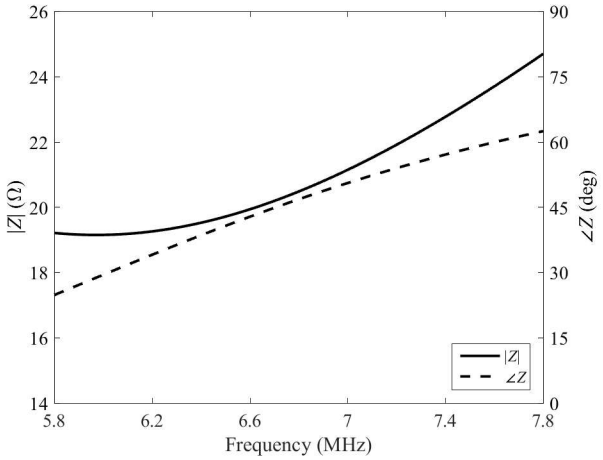

Fig. 2: Effective impedance seen by inverter.

high-frequency load into our desired impedance. Fig. 2 shows the impedance seen by the inverter with the matching network.

B. Estimated Losses and Thermal Design

The main sources of loss from the inverter are conduction loss in the resonant tank, conduction loss from the transistors, and C_{OSS} losses from the transistors. These losses cause large amounts of power to be dissipated from small areas and require careful thermal design to prevent catastrophic overheating.

1) Resonant Tank Loss: The resonant tank dissipates power primarily from the I^2R losses in the windings of the inductor. The RMS current in the inductor is approximately 8.5 A. At 6.78 MHz, typical wirewound inductors have quality factors around 200, translating to equivalent series resistances (ESR) of 0.2 Ω. If used in this inverter, such an inductor would dissipate 14 W, an amount too large to extract from a wire.

Based on this thermal consideration, we use an inductor based on a PCB toroid [9], shown below in Fig. 3. Because it is planar, we simply sandwich it between two large heat sinks (Wakefield-Vette 511-3M) with 1 mm-thick aluminum oxide ceramic plates for electrical isolation. This configuration has an estimated thermal resistance of 0.5 °C/W.

The toroid is constructed out of 2 oz copper plated on a 3.2 mm-thick FR4 board. It has 37 turns, an outer diameter of 10 cm, and an inner diameter of 4.2 cm. It has a quality factor of 110. Though the inductor dissipates twice as much power as

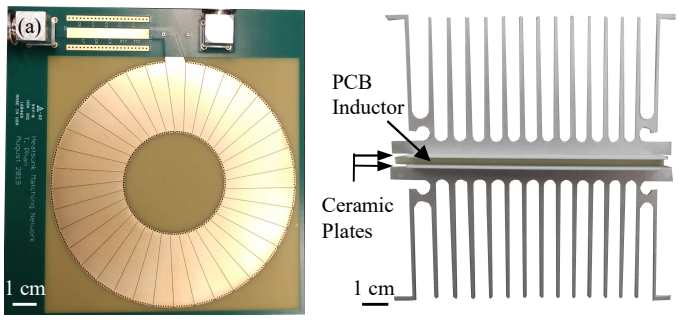

Fig. 3: PCB toroid inductor. (a) Top view, bare; (b) Side view, heatsink mounted.

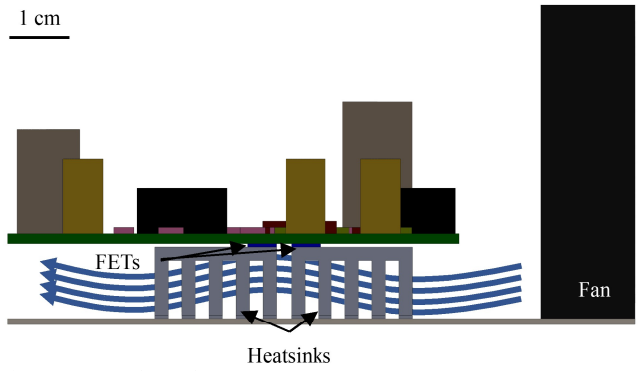

Fig. 4: Inverter thermal management system.

would a typical wirewound inductor, this is offset by the fact that it will not pose a fire hazard operating at full power.

2) Transistor Loss: Each transistor is expected to conduct an RMS current of 6 A and has an on-resistance of 80 mΩ at an estimated junction temperature of 100 °C, resulting in conduction losses of 3 W per transistor. However, the transistors also experience C_{OSS} losses [10] which are partly addressed in the manufacturer's semiconductor models. Simulations predict that each transistor will dissipate 7 W – an additional 4 W of C_{OSS} losses on top of the conduction loss.

To remove this heat, we solder heatsinks (Aavid 7109DG) directly to the transistors' thermal pads. These are then mounted on a flat surface, and a fan blows air through the channel between the board and the surface, as shown in Fig. 4. The thermal resistance is measured to be 4.5 °C/W per transistor.

C. Gate Drive and Board Layout

The transistors are driven using SiLabs SI8271 isolated gate drivers. The gate drivers provide 8 V square waves to Zener diode clamps, which constrain the applied gate voltages between -2 V and +6 V. A logic circuit on the board creates a non-overlapping clock signal with 30 ns of deadtime from a single square-wave input. Fig. 5 shows the gate drive circuit, and Fig. 6 shows the simulated gate waveforms.

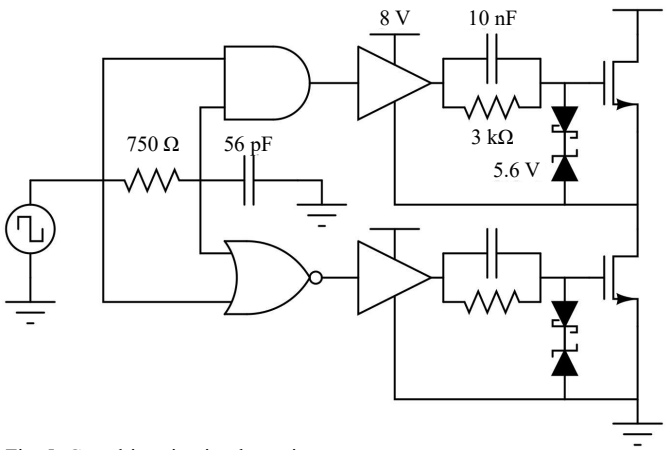

Fig. 5: Gate drive circuit schematic.

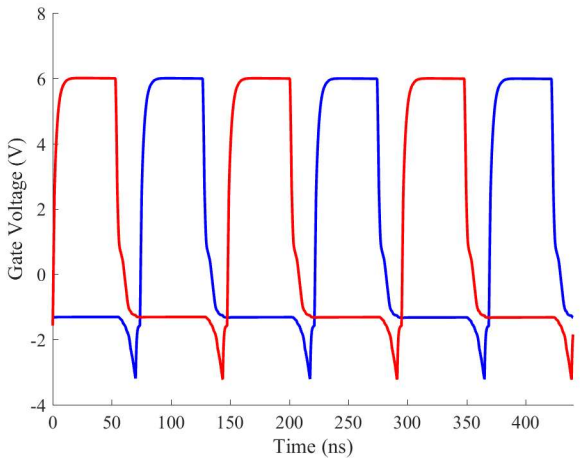

Fig. 6: Simulated inverter gate waveforms.

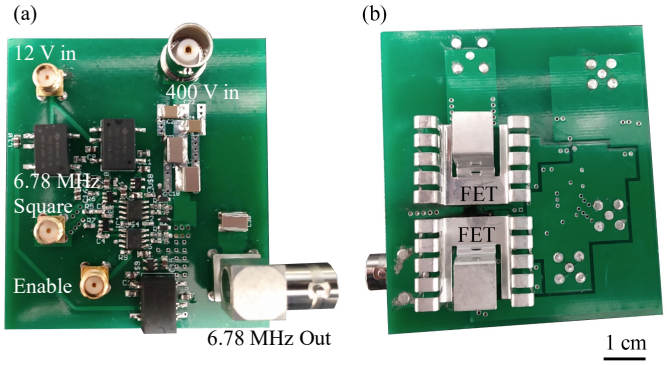

Fig. 7: (a) Top and (b) bottom views of inverter circuit board.

Fig. 7 shows the layout of the inverter circuit board. It accepts a 400 V main power supply, a 12 V supply for logic and gate drives, and a square wave input. The board measures 63 mm x 72 mm.

D. Inverter Measured Performance

The inverter draws 2.75 A of current using a 400 V supply for a total input power of 1.1 kW. The voltage waveforms at the switch node and load, shown below in Fig. 8, show that the inverter is operating under ZVS. Due to the shielded BNC

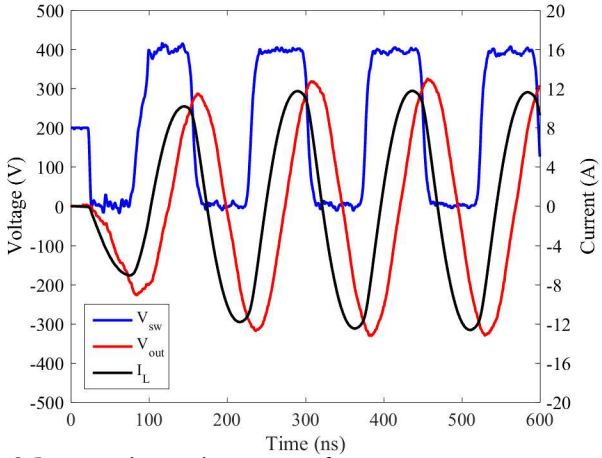

Fig. 8: Inverter voltage and current waveforms.

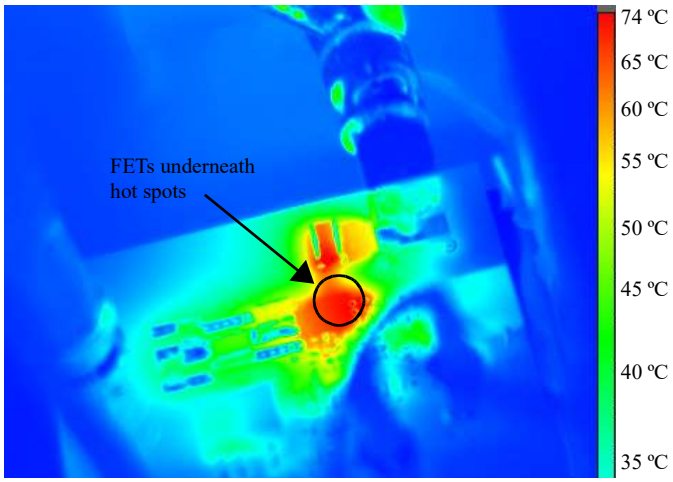

Fig. 9: Inverter thermal image under continuous operation.

connector interface, the inductor current cannot be measured directly and must be calculated from the voltages.

Fig. 9 shows an thermal image of the inverter operating continuously. The board temperature stabilizes around 74 °C, indicating that each transistor dissipates 11 W. This is much higher than the 7 W simulated losses and is likely related to unaccounted C_{OSS} losses. Since the FETs are located underneath the board, the actual junction temperature will be higher than what is shown on the image.

The PCB inductor's temperature stabilizes around 39 °C, indicating a dissipation of 34 W. These thermal measurements indicate that the inverter loses 56 W, for an output of 1.04 kW at 95% drain efficiency.

III. Wireless Link

A. Coil Construction and Electrical Characteristics

By increasing the switching frequency to 6.78 MHz, we eliminate the need for heavy litz wire and ferrites used in low-frequency designs. The coil geometry, depicted in Fig. 10, consists of a single loop of high-purity 101 copper tube 58 cm

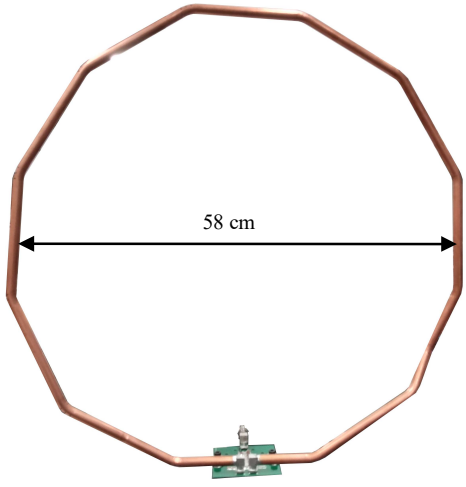

Fig. 10: Coil geometry and mounting.

in diameter (McMaster-Carr 8965K27). The loops are polygonal as the tubes were too hard to be shaped by hand and required the use of a pipe bender. These tubes have an outer diameter of 12.7 mm and wall thickness of 0.8 mm. The tubes are soldered onto female BNC connectors for mounting onto a circuit board.

A loop of this geometry has an inductance of 1.43 μH, for a reactance of $+j60.9\ \Omega$ at 6.78 MHz. The conduction resistance, accounting for the skin effect, is 31 mΩ. Large loops can also behave as antennas and lose power through radiation. The radiation resistance of a loop of diameter D can be approximated by [11]:

$$R_{rad} \approx 320\pi^4 \left(\pi \left(\frac{D}{2} \right)^2 \frac{1}{\lambda^2} \right)^2 \tag{2}$$

At 6.78 MHz, this loop has a radiation resistance of 0.6 mΩ, which is much less than the conduction resistance. With these sources of loss, the loop should have a quality factor of 1900.

The loop's self-resonant frequency (SRF) occurs when its circumference equals one quarter of a wavelength. Our loop has a circumference of 183 cm, and thus an SRF of 41 MHz. We can approximate this effect at low frequency with an equivalent parallel capacitance of 10 pF.

B. Matching Network Design

The goal of the matching network is to present the inverter with the load it was designed for in spite of the coupled inductor parasitics. This process is illustrated in Fig. 11.

The transmit and receive coils are separated by a significant gap and only exchange part of their magnetic flux. Their voltage-current relations can be expressed by an inductance matrix with k representing the inductor coupling (3). For our system, the transmit and receive coils are identical. For a separation distance of 30 cm, we expect a coupling coefficient of $k = 0.1$.

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_1 & k\sqrt{L_1 L_2} \\ k\sqrt{L_1 L_2} & L_2 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{3}$$

The cantilever transformer model [12] provides an equivalent circuit model for (3) as well as a convenient basis for incorporating the inductor parasitics into a series of L-matching networks. Four capacitors are added to the inductors in order to tune the reactances and successively transform several impedance levels.

Compared to the traditional series-resonant network [13], this method offers several advantages. The distribution of impedance transformations over several steps reduces the voltage multiplication factor on the capacitors by a factor of $\sqrt{k}$. This allows a system to transfer larger amounts of power given a particular capacitor breakdown voltage. Series-resonant networks also need large magnetizing inductances for the coils, making them heavier and requiring them to operate closer to their SRF.

Our inverter is designed for an impedance of 50 Ω, and the load has an impedance of $60 - j14\ \Omega$ (this value will be discussed in the next section). We choose intermediate impedances of 5 Ω and 500 Ω which match to the transformer coupling ratio. We can correspondingly choose the reactance values for L-matching and the required component values. At a power level of 1 kW, the highest expected voltages are approximately 1 kV. We use mica capacitors rated to 1 kV [14] and stack two in series where higher voltages are expected.

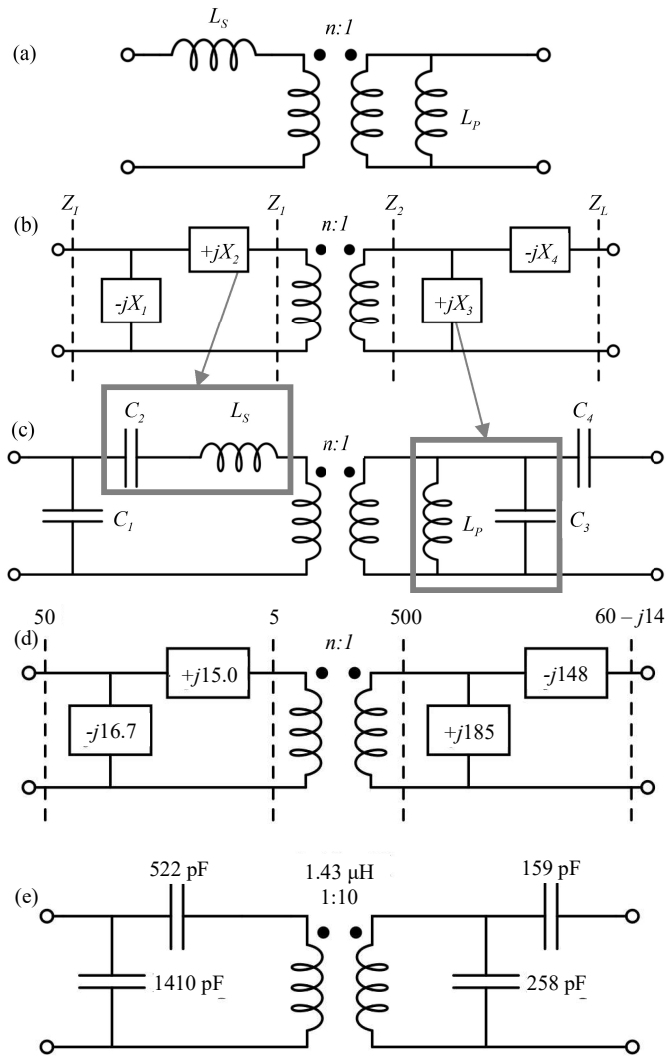

Fig. 11: Procedure for synthesizing matching network. (a) Cantilever transformer model. (b) Block diagram of impedance transformations and (c) incorporation of matching capacitors with inductor parasitics. (d) Reactance values for matching network and (e) associated component values.

With a coil quality factor of 2000 and capacitor quality factor of 3000, we expect a wireless link efficiency of 98%, with the power loss evenly split between the capacitors and coils.

C. Coil Efficiency and Impedance Measurements

The wireless link should be able to efficiently transfer power over a wide range of coil separation. We mount the coils on a set of Newport PRL optical rails to controllably vary their spacing and measure the efficiency using a network

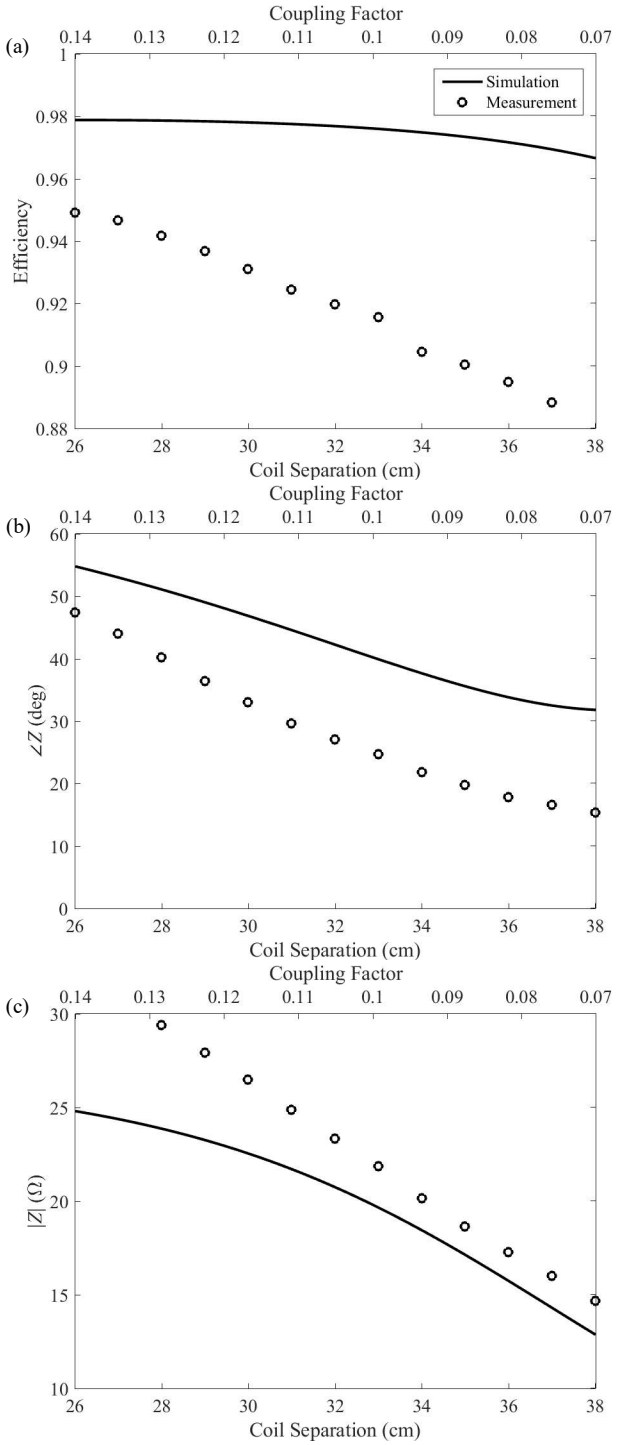

Fig. 12: Simulated and measured electrical characteristics of matched coupled coils. (a) System efficiency, (b) impedance phase, and (c) impedance magnitude as a function of separation.

analyzer, plotted in Fig. 12. The constructed system has a nominal efficiency of 92%, far less than what had been predicted by theory. We believe that about 3% of the total power is lost due to the lossy nature of the FR4 substrate, which is sustaining multi-kV voltages at 6.78 MHz. The remaining 5% is possibly due to increased coil resistance from surface oxidation and solder joint connections. The surrounding environment, such as the metallic rail and workbench, appear to have little effect on the link performance.

The wireless link also needs to present a controlled inductive load so that the inverter can operate efficiently under ZVS. This effective load impedance is also plotted in Fig. 12, and is indeed inductive while being close in magnitude to the designed value. The mismatch in simulation and measurement can be attributed to the tolerances in the capacitors.

IV. Power Rectifier

A. Filter Design

The power rectifier uses a Class-D full bridge architecture and is shown below in Fig. 13. The diodes are Cree C3D04065A SiC Schottky diodes with a 650 V, 6 A rating [15]. The rectifier uses a compact, 3-pole constant-current filter and is connected to a high-power 50 Ω load. The multi-pole filter attenuates the 13.56 MHz output ripple by 75 dB, shown in Fig. 14, without requiring large choke inductors. The 1 MHz cutoff frequency ensures that the rectifier can quickly respond to changing load conditions.

The constant-current filter serves to increase the effective load impedance, which results in less current and less conduction loss through the diodes compared to a constant-voltage filter [8]. The equivalent input impedance of the rectifier is the parallel combination of the filter load and the diodes' intrinsic capacitance:

$$Z_{eq} = \frac{\pi^2}{8} R_L \| 2C_D \tag{4}$$

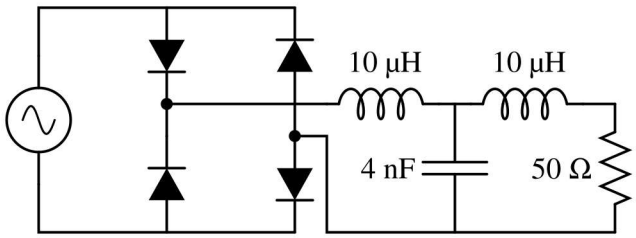

Fig. 13: Rectifier schematic.

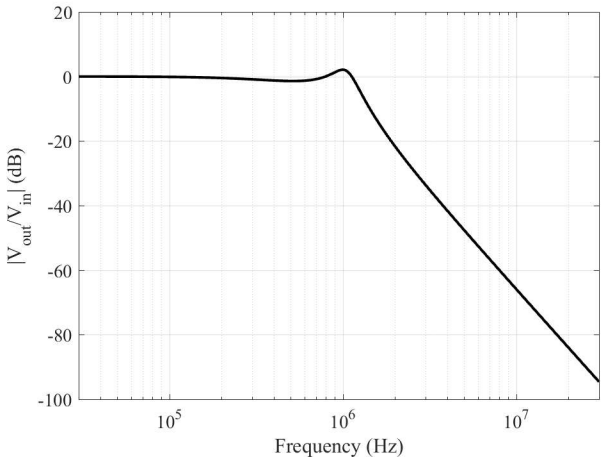

Fig. 14: Output filter frequency response.

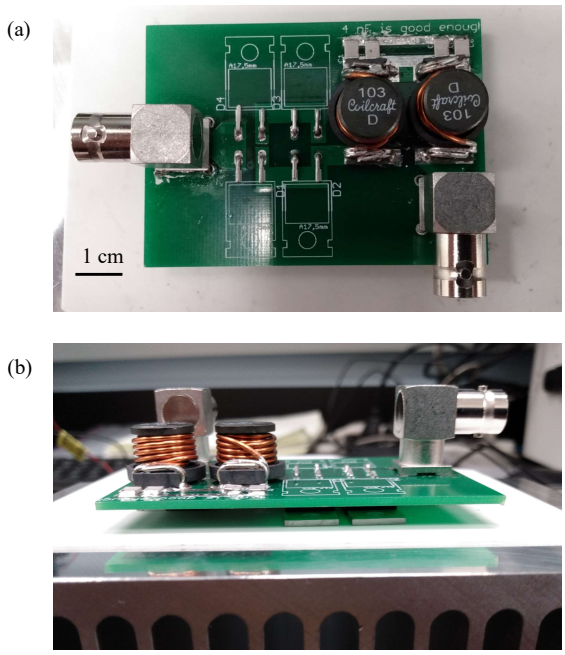

Fig. 15: (a) Top view and (b) side view of rectifier.

For our system, the equivalent impedance is Z_{eq} = 62 Ω || 90 pF, or 60 – j14 Ω at 6.78 MHz. This impedance is transformed into an inductive load through the wireless link and matching network.

B. Board Layout and Thermal Design

The rectifier is shown in Fig. 15. The diodes are mounted on the bottom of the circuit board so that they make direct contact and lie flush to the heat sink. The diodes are electrically isolated by use of a 0.4 mm-thick aluminum oxide ceramic. The measured thermal resistance is 4.4 ºC/W per diode.

The expected DC output is 1 kW, 4.5 A. Each diode should conduct 2.25 A on average, dissipate 4 W from conduction, and slightly more from output capacitance [10]. We do not expect that heating from the rectifier will be the limiting thermal factor in the DC-DC link.

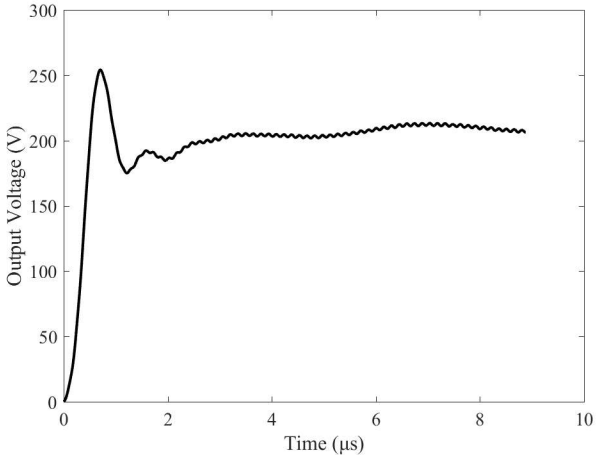

Fig. 16: Output startup transient response.

C. Transient Response

The small, multi-pole output filter allows the rectifier to respond quickly to transient conditions. We connect the inverter directly to the rectifier and view the output under startup operation, as shown in Fig. 16. The output reaches a stable DC value with a few microseconds and has a small ripple component at the switching frequency.

Unfortunately, it was not possible for us to characterize the transient response to a changing load. The electronic loads in our laboratory operate at a switching frequency below the cutoff of the rectifier filter – as a result, they do not present a stable impedance for the inverter. Attempts to deliver significant power to the electronic load resulted in catastrophic failure of the inverter.

V. Full System Measurement

The full system is shown below in Fig. 17. All subsystems are connected together by means of BNC connectors and cables. The coils are mounted on a Newport PRL optical rail system in order to accurately change their separation. Digital multimeters are used to measure the input and output voltages and currents, and therefore the system power and efficiency.

The system DC-DC power output and efficiency are plotted in Fig. 18. The efficiency is at least 75%, typically 80%, across the whole range of coil separations. Due to the inverter's parallel resonant tank, the output power actually increases as the coil separation is increased. The system is capable of delivering more than 1 kW of power to the load.

In conclusion, we demonstrate a lightweight, low-cost, robust 1 kW wireless power transfer system operating at 6.78 MHz with 82% efficiency. Further studies to determine and eliminate the losses in the wireless link, as well as incorporating the inverter's LC section directly into the wireless matching network, could dramatically improve the system's efficiency. With end-to-end efficiencies over 80% at coil separations above 30 cm, this work is an important first proof-of-concept to validate kW-scale, MHz-frequency

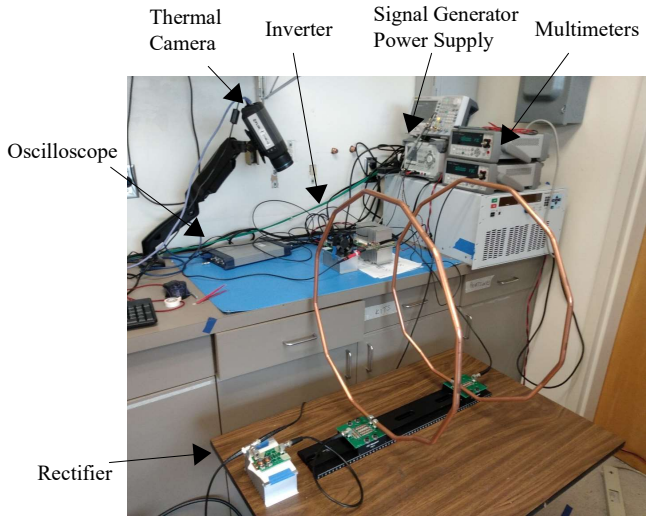

Fig. 17: Experimental measurement setup.

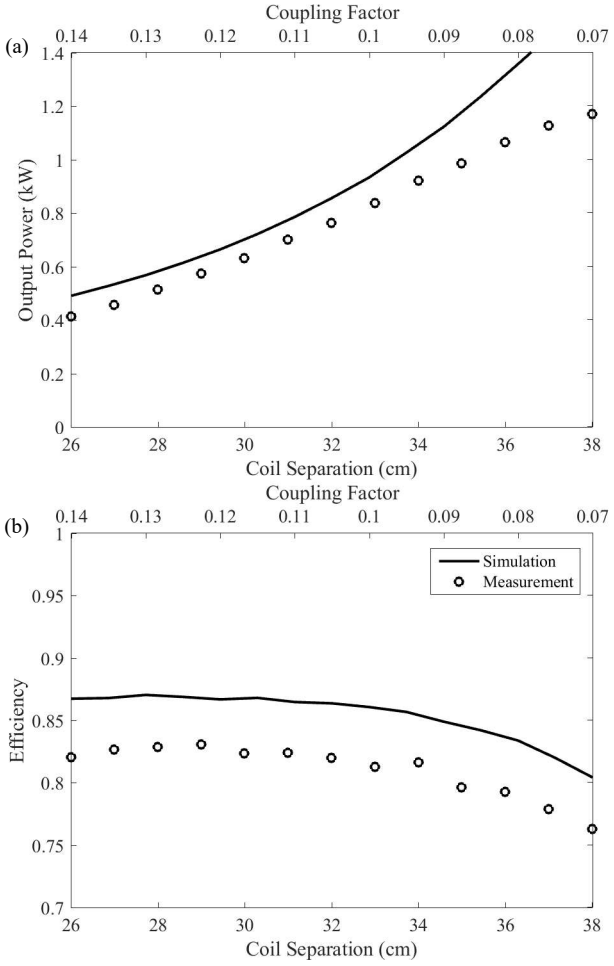

Fig. 18: Measured DC-DC (a) output power and (b) efficiency versus coil separation.

wireless charging. Further studies on thermal management and electromagnetic interference are required to scale this technology up to higher power levels.

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